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10/775,216	02/11/2004	Teruo Okada	040057	9967

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EXAMINER	
AMRANY, ADI	

ART UNIT	PAPER NUMBER
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,216	OKADA ET AL.	
	Examiner	Art Unit	
	Adi Amrany	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *29-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *29-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 35 is objected to because there is no basis for the limitation that the slave power source circuit outputs a synchronous oscillation signal via the second terminal (last two lines). The master circuit is responsible for synchronizing the slave circuits by outputting the synchronous signal; the slave circuit only inputs the signal.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 29-34, 36 and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Tominaga (US 5,237,208).

With respect to claim 29, Tominaga discloses a multiple output power source apparatus (figure 1) comprising a plurality of power source circuits (figure 1, items 1, 2, and 3, and column 5, lines 4-9) equipped with independent output control circuits (figure 2, and column 5, lines 22-26), wherein the output control circuits comprise:

a shutdown circuit (figure 2, items 34, 38; column 6, lines 9-22 and 48-52) that detects an abnormality of the own power source circuit to output an

abnormality signal to control circuits of one or a plurality of other power source circuits, and inputting an abnormality signal.

With respect to claim 30, Tominaga discloses a converter (item 26) that is driven by a switching circuit (item 31), converts an input voltage into a prescribed output voltage.

With respect to claim 31, Tominaga discloses the output stabilizing circuit (column 5, lines 50-62; column 6, lines 23-30) comprises:

a reference voltage generating circuit (item 31); an output voltage monitoring circuit (item 32); an oscillator (item 29); and a driving circuit (item 30) that controls the clock signal; and

the shutdown circuit comprises an abnormality detecting circuit (items 34, 38) that is connected to a first terminal of the other power source circuits (column 5, lines 22-26), outputs an abnormality signal when an abnormality is detected (column 6, lines 9-13), inputs an abnormality signal (column 6, lines 14-22), and stops oscillation when an abnormality is detected (column 7, lines 6-29).

With respect to claim 32, Tominaga discloses an oscillator in a master circuit is connected to an output circuit of a slave circuit via a second terminal, and outputs a synchronous oscillation signal (column 7, lines 33-42), and an oscillator in an output circuit of the slave is connected to the output circuit of the master via a third terminal, and inputs the synchronous oscillation signal from the master to perform synchronous control (column 7, lines 43-55).

With respect to claim 33, Tominaga discloses the shutdown circuit and the master/slave synchronizing, as discussed above in the rejections of claims 29 and 32, respectively.

With respect to claim 34, Tominaga discloses a converter and switching circuit (items 26, 31) and the master/slave switching signal synchronization (column 7, lines 33-55), as discussed above in the rejection of claims 30 and 32, respectively.

With respect to claim 36, Tominaga discloses a converter and switching circuit (claim 30), master/slave synchronizing (claim 32), the master circuit comprises an first oscillator, a stabilizing circuit and a shutdown circuit (claim 31), and the slave circuit comprising a second oscillator, stabilizing circuit, and shutdown circuit (claim 31), as discussed above.

With respect to claim 38, Tominaga discloses outputting the abnormality signal when a prescribed voltage is superposed on the synchronous line (figure 5; column 8, lines 5-34).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tominaga in view of Luo (US 1005/0073783).

With respect to claim 35, Tominaga discloses the converter and switching circuit (items 26, 31; claim 30), a stabilizing circuit (item 30; claim 31), a shutdown circuit (item 38; column 6, lines 1-22), and master/slave output control circuit synchronization (column 7, lines 33-55; claim 32). Tominaga does not expressly disclose that the master outputs the abnormality signal by stopping the synchronous oscillation signal.

Luo discloses a multiple output power source apparatus (figure 1; paragraph 32) comprising a plurality of power source circuits (items 10N), a stabilizing circuit (figure 1, item 22; figure 3b; paragraphs 35, 38), wherein the master outputs an abnormality signal by stopping the synchronous signal (paragraph 92, lines 5-8).

Tominaga and Luo are analogous because they are from the same field of endeavor, namely parallel power systems. At the time of the invention by applicants, it would have been obvious to one skilled in the art to combine the power source apparatus disclosed in Tominaga with the abnormality detection disclosed in Luo in order to detect the loss of a power source circuit that is not capable of actively outputting an abnormality signal.

With respect to claim 37, Tominaga discloses the shutdown circuits measure time during detection of an abnormality signal and cause the power circuit to be shut down when the measured time is a prescribed time or longer (figure 3, item 58; figure 5, item 74; column 7, lines 23-29; column 8, lines 29-34). Tominaga does not expressly disclose the master and slave circuits output the abnormality signal when the synchronous line is grounded. Luo discloses the abnormality signal is transmitted when the synchronous line is grounded, as discussed above in the rejection of claim 35.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adi Amrany whose telephone number is (571) 272-0415. The examiner can normally be reached on weekdays, from 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Sherry can be reached on (571) 272-2800 x36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AA

4/27/07